



## Integrated Differential Three-Level High-Voltage Pulser Output Stage for CMUTs

Llimos Muntal, Pere; Larsen, Dennis Øland; Jørgensen, Ivan Harald Holger; Bruun, Erik

*Published in:*

Proceedings of the 11th Conference on PhD Research in Microelectronics and Electronics (IEEE PRIME 2015)

*Link to article, DOI:*

[10.1109/PRIME.2015.7251082](https://doi.org/10.1109/PRIME.2015.7251082)

*Publication date:*

2015

*Document Version*

Peer reviewed version

[Link back to DTU Orbit](#)

*Citation (APA):*

Llimos Muntal, P., Larsen, D. Ø., Jørgensen, I. H. H., & Bruun, E. (2015). Integrated Differential Three-Level High-Voltage Pulser Output Stage for CMUTs. In *Proceedings of the 11th Conference on PhD Research in Microelectronics and Electronics (IEEE PRIME 2015)* (pp. 13-16). IEEE.  
<https://doi.org/10.1109/PRIME.2015.7251082>

---

### General rights

Copyright and moral rights for the publications made accessible in the public portal are retained by the authors and/or other copyright owners and it is a condition of accessing publications that users recognise and abide by the legal requirements associated with these rights.

- Users may download and print one copy of any publication from the public portal for the purpose of private study or research.
- You may not further distribute the material or use it for any profit-making activity or commercial gain
- You may freely distribute the URL identifying the publication in the public portal

If you believe that this document breaches copyright please contact us providing details, and we will remove access to the work immediately and investigate your claim.

# Integrated Differential Three-Level High-Voltage Pulser Output Stage for CMUTs

Pere Llimós Muntal, Dennis Øland Larsen, Ivan H.H. Jørgensen and Erik Bruun

Department of Electrical Engineering

Technical University of Denmark, Kgs. Lyngby, Denmark

plmu@elektro.dtu.dk, deno@elektro.dtu.dk, ihhj@elektro.dtu.dk, eb@elektro.dtu.dk

**Abstract**—A new integrated differential three-level high-voltage pulser output stage to drive capacitive micromachined ultrasonic transducers (CMUTs) is proposed in this paper. A topology comparison between the new differential output stage and the most commonly used single-ended topology is performed in order to assess the performance of the new output stage. The new topology achieves a 10.9% lower power consumption and an area reduction of 23.5% for the same specifications. The differential output stage proposed is able to generate pulses with a slew rate of 2 V/ns, a frequency of 5 MHz and voltage levels of 60, 80, 100 V using 0.039 mm<sup>2</sup> of chip area. The power consumption is 0.951 mW for a 30 pF CMUT load. The design presented is implemented in a 0.35  $\mu$ m high-voltage process.

## I. INTRODUCTION

Pulse generators with voltage levels up to 100 - 200 V (from here on referred as pulsers) are widely used in applications such as medical ultrasound imaging, B-scan ultrasound, non-destructive ultrasound material flaw detection, sonar transmitters and signal generation in test instruments. A principle diagram of a high-voltage pulser can be seen in Fig. 1. The logic block generates low-voltage signals which are converted into high-voltage by the level shifter block obtaining the control signals for the switches in the output stage [1]. The output stage is the main focus of this paper since it is typically the biggest and most power consuming block, hence its optimization is a key factor to minimize the overall power consumption and area of the pulser. Integrating the output stage reduces the area utilized to implement the circuit and also reduces the power consumption, compared to the implementation with discrete components. However, voltages up to 100 V can not be handled with standard CMOS processes, therefore a high-voltage process is needed. Using a high-voltage process has an impact on the design of the output stage since such processes are significantly different from standard CMOS ones. High-voltage processes have more design rules and restrictions and they also use high-voltage devices which are bigger and have more complex structures

than standard devices due to larger isolation distances required to avoid voltage breakdowns.

Minimizing the power consumption and area of the output stage is specially relevant in applications like hand-held ultrasound scanners where arrays of thousands of transducers need to be driven, and each of them requires an output stage. The capacitive micromachined ultrasonic transducers (CMUTs) used in these scanners consist of a thin plate suspended on top of a substrate with a vacuum gap in between that allows the plate to vibrate. These transducers have two terminals, one connected to the plate and the other connected to the substrate, and by applying a voltage difference between terminals, the transducer is able to generate ultrasound. A high bias voltage is needed in order to receive and high-voltage pulses at a frequency in the order of a few megahertz are required in order to transmit [2]. Both the high bias voltage and the high voltage pulses are provided by the output stage. An inherent advantage of CMUTs is that they can be directly built on the top of an electronic wafer saving area and interconnection capacitances [3]. The design of an output stage for CMUTs is especially challenging since it needs both high speed and high voltage, which are usually very strict requirements. Furthermore, the pulses to transmit need to be symmetrical with respect to the bias voltage in order to achieve high quality signals from the CMUT, therefore three voltage levels are required from the output stage.

In this paper a new integrated differential three-level high-voltage pulser output stage topology to drive CMUTs is presented and implemented in a 0.35  $\mu$ m high-voltage process. An output stage topology comparison between the new differential output stage and the most commonly used single-ended output stage [4] is performed in order to assess the performance of the new topology proposed. The power consumption of an output stage depends on the pulse shape generated, however in this paper a method that allows the designer to compare the topologies for any type of pulse shape is presented and used.

## II. OUTPUT STAGE SPECIFICATIONS

In order to compare the different output stage topologies, they must meet the same specifications. The type of transducer to drive, the characteristics of the output pulse and the process are defined in this section.

Firstly, the transducer to be driven is assumed to be a CMUT with a capacitance of 30 pF, a resonant frequency of 5 MHz and a bandwidth up to 15 MHz. CMUTs are non-

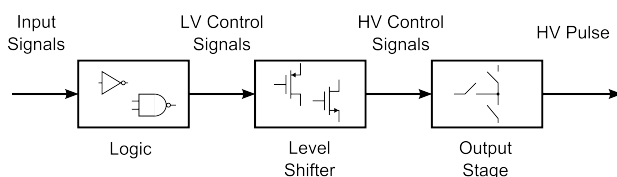


Fig. 1. Structure of a high-voltage pulser.

polarized devices that require a high bias voltage when receiving and a symmetrical pulse with a frequency matching the resonant frequency of the CMUT when transmitting. The three voltage levels needed between terminals of the transducer are specified at 60 V, 80 V and 100 V, where 80 V is the bias voltage of the CMUT in receiving mode.

The slew rate (SR) of the pulses that the output stage needs to generate is set by the maximum frequency response of the CMUT, which is the 15 MHz bandwidth, and the voltage swing of the pulse, which corresponds to an amplitude of 20 V. Assuming a sinusoidal signal of the before-mentioned characteristics, its derivative in time leads to the change of voltage per unit time (1). The maximum of this function defines the SR of the transducer (2) which sets the SR requirement for the output stage. Based on this analysis, the output stage is designed to have a SR of 2 V/ns.

$$\frac{dV_{sin}}{dt} = \frac{dA \sin(2\pi ft)}{dt} = 2\pi Af \cos(2\pi ft) \quad (1)$$

$$\max[2\pi Af \cos(2\pi ft)] = 2\pi Af = 1.885 \text{ V/ns} \quad (2)$$

For the implementation a 0.35  $\mu\text{m}$  high-voltage process is used, which can handle a maximum voltage difference from any point of the circuit to the substrate of 120 V hence it can accommodate the highest voltage of the design (100 V).

### III. COMPARISON PROCESS

The new differential topology and the commonly used single-ended topology are compared by power consumption, area of the devices and other specific topology considerations.

#### A. Power consumption expression

Accounting for the power consumption of a three-level output stage is not a trivial task since it depends on the pulse shape generated by it and its period. The approach proposed in this paper provides a method to compare the power consumption of different topologies for any type of pulse shape and period. The idea is to find a generic expression that yields the power consumption for a given pulse shape and period and then easily evaluate in any particular case. The process to derive this expression is explained below. A generic pulse with three voltage levels,  $V_L$ ,  $V_M$  and  $V_H$ , is shown in Fig. 2. As it can be seen, three voltage levels correspond to six different voltage transitions,  $tr_j$  ( $j \in [1, 6]$ ). From now on any pulse shape is characterized by its total period,  $T$ , and the number of each  $tr_j$  transitions,  $N_j$ . It is worth to notice that  $T$  is not the period of the pulses  $T_P$ , but the overall periodicity of the

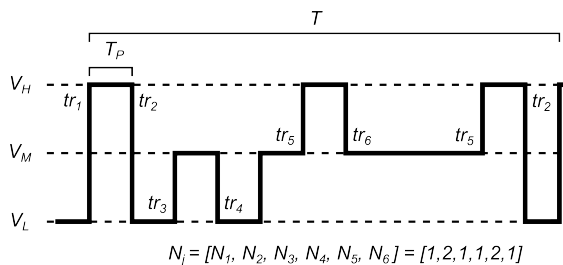


Fig. 2. Pulse with three voltage levels characterized by  $T$  and  $N_j$ .

signal. The fundamental frequency of the transmitting pulses  $f_p = T_P^{-1}$  is assumed to be a maximum of 5 MHz which is the resonant frequency of the CMUT defined in section II. In order to consider every pulse shape, the energy needed for each transition  $tr_j$  needs to be found. Assuming  $K$  number of voltage supplies needed to generate the pulses, the charge  $Q_{i,j}$  required from the voltage supply  $V_i$  ( $i \in [1, K]$ ) for the transition  $tr_j$  is found by integrating the current flowing from it during that transition (3). The total energy  $E_j$  needed for the transition  $tr_j$  is found by multiplying  $Q_{i,j}$  of each supply by its voltage  $V_i$ , and adding them all together (4). The total power consumption of a pulse characterized by  $T$  and  $N_j = [N_1, N_2, N_3, N_4, N_5, N_6]$  can be obtained by combining these characteristics with the energy required for each type of transition  $E_j$  using equation (5). This equation will be used to compare the power consumption of the topologies for any pulse shape. The total energy required for each type of transition,  $E_j$ , needs to be found by extracting all the  $Q_{i,j}$  from simulations.

$$Q_{i,j} = \int I_i(t) dt, \quad \forall i \in [1, K] \quad \forall j \in [1, 6] \quad (3)$$

$$E_j = \sum_{i=1}^K V_i Q_{i,j} = \sum_{i=1}^K V_i \int I_i(t) dt, \quad \forall j \in [1, 6] \quad (4)$$

$$P_{T,N_j} = \frac{1}{T} \sum_{j=1}^6 N_j E_j = \frac{1}{T} \sum_{j=1}^6 N_j \sum_{i=1}^K V_i \int I_i(t) dt \quad (5)$$

#### B. MOS devices characteristics

In the 0.35  $\mu\text{m}$  high-voltage process used, there are different high-voltage MOSFET devices. These devices are more complex and bigger than the standard CMOS process ones, since they require different types of isolation like grounded guard-rings around them. These devices are mainly differentiated breakdown gate-source voltage and breakdown drain-source voltage. The high-voltage process used contains devices with different voltage breakdown options and the relevant ones for the design are shown in Fig.3. As it is expected, the size and parasitics of the device increases significantly with its voltage breakdown capabilities affecting negatively the area and power consumption of the circuitry. Consequently, in high-voltage circuit design, the MOS transistors with the lowest breakdown voltages that satisfy the specifications are selected. For this reason MOS transistors with a  $V_{gs,max} = 5 \text{ V}$  are chosen. During the comparison, the area of each topology is accounted including the required guard-rings of each device.

### IV. TOPOLOGIES AND SIMULATIONS

Two topologies are designed to meet the specifications defined in section II. Firstly, the type of each high-voltage

Symbol								
Type	PMOS	PMOS	NMOS	NMOS	NMOS	PMOS	NMOS	NMOS
$ V_{ds,max} $ [V]	50	50	50	50	50	20	20	20
$ V_{gs,max} $ [V]	20	5.5	20	5.5	5.5	5.5	5.5	5.5

Fig. 3. Sample of MOS devices available in the high-voltage process. NMOS states for isolated NMOS transistors.

TABLE I. CHARGE AND ENERGY PER TRANSITION, SINGLE-ENDED

	$Q_{V_{20}}$ [nC]	$Q_{V_{40}}$ [nC]	$Q_{V_{100}}$ [nC]	Energy [nJ]
60→100 V	0.0157	-0.0006	1.3600	136.29
100→60 V	-0.0093	1.4200	-1.3590	-79.29
60→80 V	-0.7183	-0.0052	0.6654	51.97
80→60 V	-0.2254	0.9617	-0.6793	-33.97
80→100 V	0.0302	0.0046	0.6797	68.76
100→80 V	0.7153	-0.0044	-0.6674	-52.61

device is chosen according to its  $V_{gs,max}$  and  $V_{ds,max}$ . Secondly, the width and length of the devices are adjusted in order to achieve a minimum  $|SR| = 2 \text{ V/ns}$  for each voltage transition  $tr_j$ . Afterwards the energy required for each voltage transition  $tr_j$  is found as explained in subsection III-A. Finally, the devices are laid-out and the total area is measured. For the simulations, an electrical CMUT model derived from a fabricated CMUT of the previously specified characteristics is connected to the different output stage topologies in order to provide results closer to the real operation of the pulser. Consequently, the power consumption obtained will contain both the power to charge and discharge the CMUT and the power to charge and discharge the parasitic capacitances of the corresponding output stage. The fabrication of the transducer and the electrical model extraction have been done at DTU Nanotech, however the schematic of the model is confidential so it is not included in this paper.

#### A. Three-level single-ended Output Stage

The topology presented in this section is a single-ended output stage, which is the most commonly used [4]. Since CMUT transducers are non-polarized devices, an inherent advantage of this topology is that the pulser is connected to only one terminal of the transducer, hence the other terminal can be used to apply an external high bias voltage [5]. The voltage level between terminals of the transducer are specified at 60 V, 80 V and 100 V, however, by biasing one of the terminals of the transducer to 100 V, the output stage is only required to generate voltage levels of 0 V, 20 V and 40 V. The schematic of the three-level single-ended output stage is shown in Fig. 4. Transistors  $M_1$ ,  $M_2$ ,  $M_{3-4}$  function as switches connecting the output voltage to  $V_1 = 40 \text{ V}$ ,  $V_2 = 0 \text{ V}$  and  $V_{3,4} = 20 \text{ V}$  respectively. The main problem of this topology is that three different voltage levels are connected to a single output node, which leads to the need of two different switches

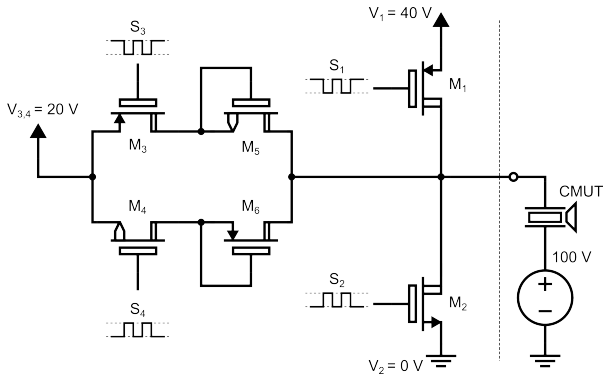


Fig. 4. Three-level single-ended output stage schematic.

TABLE II. CHARGE AND ENERGY PER TRANSITION, DIFFERENTIAL

	$Q_{V_{20}}$ [nC]	$Q_{V_{80}}$ [nC]	$Q_{V_{100}}$ [nC]	Energy [nJ]
60→100 V	-0.0100	0.0702	1.3410	139.52
100→60 V	1.3760	-1.4040	-0.0057	-85.37
60→80 V	-0.0282	0.7013	0.0000	55.54
80→60 V	0.7149	-0.6793	0.0000	-40.04
80→100 V	-0.0028	0.0099	0.7217	72.91
100→80 V	0.0020	-0.7243	-0.0064	-58.54

connected to  $V_{3,4}$  ( $M_3$  and  $M_4$ ) in order to be able to pull down from  $V_1$  or pull up from  $V_2$ . It also adds the requirement of two extra transistors used as diodes,  $M_5$  and  $M_6$ , to avoid short circuiting  $V_1 - V_{3,4}$  through the body diode of  $M_3$  when the output voltage is  $V_1$  and  $V_2 - V_{3,4}$  through the body diode of  $M_4$  when the output voltage is  $V_2$ . Note that both  $M_1$  and  $M_2$  require a  $V_{ds,max} = 50 \text{ V}$  whereas all the other transistors only require  $V_{ds,max} = 20 \text{ V}$ . Minimum lengths of  $1 \mu\text{m}$  for PMOS and  $0.5 \mu\text{m}$  for NMOS are used for all devices to minimize the parasitic capacitances. The energy required for each voltage transition is shown in table I.

#### B. Three-level differential Output Stage

The new differential output stage topology presented in this paper is described in this subsection. The schematic of this output stage can be seen in Fig. 5. It consists of two two-level output stages where the output node of each of them is connected to one of the terminals of the transducer obtaining differential driving. However, now both terminals of the transducer are connected to the output stage, therefore the CMUT can not be connected to high bias voltage in one of the terminals anymore. Since the CMUT is floating, now the high bias voltage needs to be implemented in the output stage using non-symmetrical voltage levels in the two two-level output stages.  $V_1$ ,  $V_2$ ,  $V_3$  and  $V_4$  are set to 100 V, 80 V, 20 V and 0 V respectively. The specified voltage levels between the terminals of the CMUT of 100, 80 V and 60 V are achieved by turning on  $M_{1,4}$ ,  $M_{2,4}$  or  $M_{1,3}$  and  $M_{2,3}$  correspondingly. In spite of its higher voltage levels, this topology solves the problem of the single-ended topology of having three different voltage levels in one single output node therefore. Consequently, there is no need of any extra transistors to avoid short circuits which reduces the area of the output stage. Furthermore, since the pulse voltage swing is split in two sides, the maximum  $V_{ds,max}$  that the MOS devices need to handle is only 20 V

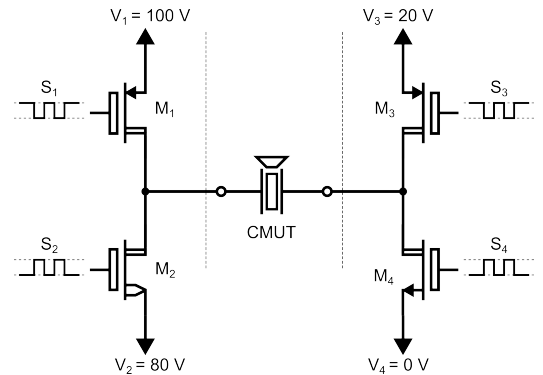


Fig. 5. Three-level differential output stage schematic.

hence smaller devices than the single-ended version can be used reducing the area even further. The parasitic capacitances of the MOS devices are also reduced so a power consumption reduction is also expected. The differential driving with non-symmetrical voltages is possible due to the capacitive nature of CMUTs, which isolates the DC voltages of each two-level output stage from each other. Using the same reasoning as the single-ended output stage, the devices are again sized with minimum length, and the energy required for each voltage transition is shown in table II.

## V. RESULTS AND DISCUSSION

Using (5) and the energies in table I and II the power consumption  $P_{T,N_j}$  [mW] as a function of the period,  $T$  [μs], and the number of transitions per period,  $N_j$ , is shown in (6) and (7) for the single-ended and differential output stages respectively. Using these equations, the power consumption of any pulse shape can be found for both topologies. In order to have a qualitative idea of the power consumption of both output stages, eight common pulse shapes to drive CMUTs are inserted in equations (6) and (7). In all of these cases, the differential output stage proves to be the least power consuming one. However, the power consumption difference between topologies varies depending on the pulse shape from a small improvement of 4.3% to a significant reduction of 17.7%. The characteristics of the pulse used to drive the CMUTs in an ultrasound scanner are  $T=100\mu s$  and  $N_j=[2,1,0,1,0,1]$ . The power consumption associated to that specific pulse shape is 1.067 mW for the single-ended topology and 0.951 mW for the differential topology, which is 10.9% lower. The power consumption reduction is attributed to the expected lower parasitic capacitances in the differential output stage.

$$P_{T,N_j}|_{se} = \frac{1}{T}(136.29 \cdot N_1 - 79.29 \cdot N_2 + 51.97 \cdot N_3 - 33.97 \cdot N_4 + 68.76 \cdot N_5 - 52.61 \cdot N_6) \quad (6)$$

$$P_{T,N_j}|_{diff} = \frac{1}{T}(139.52 \cdot N_1 - 85.37 \cdot N_2 + 55.54 \cdot N_3 - 40.04 \cdot N_4 + 72.91 \cdot N_5 - 58.54 \cdot N_6) \quad (7)$$

The area of both topologies is accounted by adding the area of all the devices obtaining 0.051 mm<sup>2</sup> for the single-ended and 0.039 mm<sup>2</sup> for the differential. The area of the differential output stage is 23.5% smaller than the single-ended mainly due to fewer number of transistors. However, the differential stage requires one more output pad, which should also be accounted for in the area. Nonetheless, both output stage topologies designed have an inherent ESD protection due to the large size of the devices and their body diodes. The aforementioned inherent ESD protection has been previously tested and proven to be sufficient hence only an extra pad opening of 0.025 mm<sup>2</sup> placed directly on the top of the output stage would be required, occupying no extra area [6].

There are other aspects to consider apart from the power consumption and area of the two topologies. Firstly, in the single-ended output stage, the transistors  $M_5$  and  $M_6$ , used as diodes, generate a small voltage drop that causes a small offset from the middle voltage level in the output node. If accurate voltage levels are required to drive the output, the differential output stage would be preferred. Secondly, it is worth to notice that, in the differential topology, by applying non symmetrical

TABLE III. TOPOLOGY COMPARISON FOR A 30 pF CMUT LOAD

	A [mm <sup>2</sup> ]	P [mW]
Single-ended	0.051	1.067
Differential	0.039	0.951
Comparison	-0.012 (-23.5%)	-11.6 (-10.9%)

voltage differences  $V_1$ - $V_2$  and  $V_3$ - $V_4$  a fourth voltage level can be achieved. Further research will analyze the advantages of using a fourth level and its effect on the power consumption and circuit performance.

For a generated pulse characterized by  $T=100\mu s$  and  $N_j=[2,1,0,1,0,1]$  and a sufficient inherent ESD protection from the output stages, the comparison between two topologies is shown in table III. The differential output stage is the smallest and the lowest power consuming. The area and power savings correspond to 0.012 mm<sup>2</sup> and 0.116 mW. It is important to consider that in ultrasound scanners transducers, arrays of hundreds of transducers and output stages are required, therefore the area and power savings of the differential topology become even more significant. The comparison can easily be remade for any other pulse shape using equations (6) and (7).

## VI. CONCLUSION

In this paper a new integrated differential three-level high-voltage pulser output stage is implemented and presented. The new differential topology is compared to the typical single-ended output stage optimizing them to drive a 30 pF CMUT with a frequency of 5 MHz and a SR of 2 V/ns and implementing them in a 0.35 μm high-voltage process. The comparison shows that the new differential topology is the smallest and the least power consuming. A total chip area of 0.039 mm<sup>2</sup> and a power consumption of 0.951 mW is achieved using the differential topology saving 23.5% of area and 10.9% of power from the single-ended output stage. The differential output stage is tapped out in a 0.35 μm high-voltage process, and the integrated circuit will be measured after fabrication.

## REFERENCES

- [1] Dongning Zhao, Meng Tong Tan, Hyouk-Kyu Cha, Jinli Qu, Yan Mei, Hao Yu and Arindam Basu, Minkyu Je, "High-voltage Pulser for Ultrasound Medical Imaging Applications" in *International Symposium on Integrated Circuits*, 2011, pp.408-411.
- [2] Arif. S.Ergun, Goksen G. Yarioluglu and Butrus T. Khuri-Yakub, "Capacitive Micromachined Ultrasonic Transducers: Theory and Technology" in *Journal of Aerospace Engineering*, 2013, pp.74-87.
- [3] G. Gurun, P. Hasler and F.L. Degertekin, "Front-End Receiver Electronics for High-Frequency Monolithic CMUT-on-CMOS Imaging Arrays" in *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control*, 2011, Vol. 58, No. 8, pp.1658-1668.
- [4] K. Chen, H-S. Lee, A.P. Chandrakasan and C.G. Sodini, "Ultrasonic Imaging Transceiver Design for CMUT: A Three-Level 30-Vpp Pulse-Shaping Pulser With Improved Efficiency and a Noise-Optimized Receiver" in *IEEE Journal of Solid-State Circuits*, 2013, Vol. 48, No. 11, pp.2734-2745.
- [5] I.O. Wygant, X. Zhuang, D.T. Yeh, A. Nikoozadeh, . Oralkan, A.S. Ergun, M. Karaman and B.T. Khuri-Yakub, "An Endoscopic Imaging System Based on a Two-Dimensional CMUT Array: Real-Time Imaging Results" in *IEEE Ultrasonic Symposium*, 2005, pp.792-795.
- [6] I.O. Wygant, X. Zhuang, D.T. Yeh, . Oralkan, A.S. Ergun, M. Karaman and B.T. Khuri-Yakub, "Integration of 2D CMUT Arrays with Front-End Electronics for Volumetric Ultrasound Imaging" in *IEEE transactions on ultrasonics, ferroelectrics, and frequency control*, 2008, Vol. 55, No. 2, pp.327-342.